What is claimed is:

1. A method of forming a shallow-trench-isolation structure in a silicon integrated-circuit wafer, comprising:

   a. providing a silicon wafer having a (100) crystallographic top surface and a bottom surface;

   b. providing a indicating means on the wafer of a [100] crystallographic direction;

   c. forming an approximately 100Å thick pad silicon-oxide layer on the top surface;

   d. forming an approximately 1,200Å thick silicon-nitride layer on the silicon-oxide layer;

   e. forming a photo-resist layer on the silicon-nitride layer;

   f. forming a shallow-trench-isolation (STI) pattern in the photo-resist layer, uncovering a portion of the top surface, the STI pattern having trench-edges aligned, within 10 degrees, to the <100> crystallographic directions of the silicon wafer;

   g. etching a portion of the silicon-nitride layer uncovered by the STI pattern, uncovering a portion of the pad silicon-oxide layer;

   h. etching the portion of the pad silicon-oxide layer uncovered by the nitride layer, uncovering a portion of the silicon wafer;

   i. removing the photo-resist layer from the surface of the wafer;

   j. etching the portion of the silicon wafer uncovered by the pad silicon-dioxide layer to form a trench with sidewalls, a portion of the sidewall near the top surface is within 15 degrees of being perpendicular to the top wafer-surface;

   k. removing a portion of the pad oxide layer to uncover a portion of the silicon surface near the sidewall by dipping the wafer in dilute hydro-fluoric acid;

l. growing a silicon-dioxide-liner layer on the uncovered silicon top surface and on the trench-sidewalls and on corners where sidewall surfaces approach the top surface, the growth being in a oxidation furnace at about 850°C, the liner-oxide layer at the corner being over 50% thicker than at the sidewall adjacent to the corners; and

m. filling the trench with silicon dioxide material.

2. The method of claim 1 in which the silicon wafer contains an approximately 20% germanium-doped silicon layer near the top surface.

3. A method of forming a trench structure in a wafer of semiconductor material, comprising:

   a. providing a semiconductor wafer having a top surface that has a oxidization rate slower than that of other major crystallographic planes of the semiconductor material;

   b. etching a portion of the silicon wafer according to a trench pattern, forming substantially vertical trench-sidewalls near the top surface, the vertical trench-sidewalls near the top surface containing crystallographic plane that oxidizes at a rate comparable to that of the top surface; and

   c. growing an insulating layer on the top surface and on the trench-sidewalls and on corners where sidewall surfaces approach the top surface, the insulating layer at the corners being substantially thicker than at the sidewall adjacent to the corners; and

   d. filling the trench with a dielectric material.

4. The method of claim 3, in which the semiconductor is silicon.

5. The method of claim 4, in which the silicon contains a germanium doped layer near the top surface.

6. The method of claim 5, in which the concentration of the germanium dopant is about 20%.

7. The method of claim 4, in which the top surface contains a (100) crystallographic plane.

8. The method of claim 4, further comprising a pad oxide layer and a nitride layer on the wafer surface.

9. The method of claim 8, in which the pad oxide is approximately 100Å thick and the nitride layer is approximately 1,200Å thick.

10. The method of claim 3, in which the trench pattern comprises a photo-resist pattern.

11. The method of claim 4, in which the top portion of the sidewalls contain {100} planes.

12. The method of claim 3, in which the sidewalls are within 10 degrees to vertical to the top surface.

13. The method of claim 4, in which the corners uncover crystallographic planes other than {100} planes.

14. The method of claim 4, in which the insulating material is silicon dioxide thermally grown on the sidewalls and the top surface.

15. The method of claim 14, in which the grown dioxide at the corners is at least 1.5 times thicker than the grown dioxide layer at the top portion of the sidewalls.

16. The method of claim 4, in which the growing of the insulating layer is at a temperature below 900°C.

17. The method of claim 4, in which the growing of the insulating layer is at approximately 850°C.

18. A trench structure in a wafer of semiconductor material, comprising:

a. a semiconductor wafer having a top surface that has a oxidization rate slower than that of other major crystallographic planes of the semiconductor material;

b. a trench structure with substantially vertical trench-sidewalls near the top surface, the vertical trench-sidewalls near the top surface containing crystallographic plane that oxidizes at a rate comparable to that of the top surface; and

c. an insulating layer on the top surface and on the trench-sidewalls and on corners where sidewall surfaces approach the top surface, the insulating layer at the corners being substantially thicker than at the sidewall adjacent to the corners; and

d. the trench filled with a dielectric material.

19. The trench structure of claim 18, in which the semiconductor material is silicon.

20. The trench structure of claim 19, in which the silicon contains a germanium doped layer near the top surface.

21. The trench structure of claim 20, in which the concentration of the germanium dopant is about 20%.

22. The trench structure of claim 19, in which the top surface contains a (100) crystallographic plane.

23. The trench structure of claim18, further comprising a pad oxide layer and a nitride layer on the wafer surface.

24. The trench structure of claim 23, in which the pad oxide is approximately 100Å thick and the nitride layer is approximately 1,200Å thick.

25. The trench structure of claim 18, in which the trench pattern comprises a photo-resist pattern.

26. The trench structure of claim 19, in which the top portion of the sidewalls contain {100} planes.

27. The trench structure of claim 18, in which the sidewalls are within 10 degrees to vertical to the top surface.

28. The trench structure of claim 19, in which the corners uncover crystallographic planes other than {100} planes.

29. The trench structure of claim 19, in which the insulating material is silicon dioxide thermally grown on the sidewalls and the top surface.

30. The trench structure of claim 29, in which the grown dioxide at the corners is at least 1.5 times thicker than the grown dioxide layer at the top portion of the sidewalls.

31. The trench structure of claim 29, in which the silicon dioxide is formed at a temperature below 900 °C.

32. The trench structure of claim 29, in which the silicon dioxide is formed at a temperature of approximately 850 °C.